PATENT CLAIMS

1. An optoelectronic sensor comprising at least one photodiode (1) which can be connected to a first potential (V_{reset}, V_{reset1}) via a first transistor (T1) or a first diode (D1),
characterized in that
in order to provide a large dynamic range, the photodiode (1) can furthermore be connected to the input of a readout amplifier (T3) via a second transistor (T2), a third transistor (T5) via which the input of the readout amplifier (T3) can be connected to a second potential (V_{reset}, V_{reset2}) furthermore being arranged between the second transistor (T2) and the input of the readout amplifier (T3), and
in that there are means (C2) which allow temporary storage of the integrated signal value until the readout time.

2. The optoelectronic sensor as claimed in claim 1, characterized in that there is a first transistor (T1), and in that the first and second potentials (V_{reset}) are at an essentially identical voltage level.

3. The optoelectronic sensor as claimed in one of the preceding claims, characterized in that an additional conversion node capacitor (C2) to ground potential (2) is arranged between the second transistor (T2) and the input of the readout amplifier (T3).

4. The optoelectronic sensor as claimed in one of the preceding claims, characterized in that the output of the readout amplifier (T3) is connected to a column bus via a row selection transistor (T4).

5. The optoelectronic sensor as claimed in one of the preceding claims, characterized in that at least one, and preferably all of the transistors (T1, T2, T3, T4, T5) used are designed as MOS transistors.

6. The optoelectronic sensor as claimed in one of the preceding claims, characterized in that the gate voltage of the second transistor (T2) is controlled so that the current generated by the photodiode (1) discharges only a capacitor (C2) at the input of the

readout amplifier (T3) in a first phase of the integration time, and in that the gate voltage of the first transistor (T1), or respectively the first potential (V_{reset1}) when there is a first diode (D1), is in this case controlled so that some or all of the current generated by the photodiode (1) is compensated for by the channel of the first transistor (T1) or respectively by the first diode (D1) in a last phase of the integration time.

7. The optoelectronic sensor as claimed in claim 6, characterized in that in the case of a first transistor (T1) the gate voltage of the first transistor (T1) is lower than the gate voltage of the second transistor (T2) and in that the gate voltage of the first transistor (T1) is higher than the saturation signal of the readout buffer at least by a threshold voltage, or respectively in that in the case of a first diode (D1) the diode anode voltage of the first diode (D1) is adjusted by the first potential (V_{reset1}) so that this anode voltage minus the diode threshold voltage ($V_{reset1} - V_{onDiode}$) is lower than the gate voltage minus the threshold voltage of the second transistor (T2) and in that the diode anode voltage (V_{reset1}) of the first diode (D1) is higher than the saturation signal of the readout buffer at least by a diode threshold voltage ($V_{onDiode}$).

8. The optoelectronic sensor as claimed in claim 6, characterized in that the difference between the two gate voltages is greater than the tolerance of the threshold voltages plus the tolerance of the voltage values, this difference particularly preferably being selected to be > 100 mV.

9. The optoelectronic sensor as claimed in one of the preceding claims, characterized in that the gate voltages of the first transistor (T1) and of the second transistor (T2) can be varied during the integration time.

10. A method for operating an optoelectronic sensor as claimed in at least one of claims 1 to 9,

characterized in that the gate voltage of the first transistor (T1), or respectively the first potential (V_{reset1}) in the case of a first diode (D1), and the gate voltage of the second transistor (T2), is respectively adjusted or controlled so that charge carriers accumulated by the photodiode (1) discharge only a conversion node capacitor (C2) in a first phase of the integration time, in that charge carriers accumulated by the photodiode (1) discharge both a photodiode capacitor (C1) and said conversion node capacitor (C2) in a second phase after an equal potential has been reached at the output of the photodiode (1) and at the input of the readout amplifier (T3), and in that after the output of the photodiode (1) has fallen below the threshold value of the first transistor (T1) or respectively the diode threshold value of the first diode (D1), charge carriers accumulated by the photodiode (1) are at least partially made available via the first transistor (T1) or respectively via the first diode (D1) in a third phase, and in that said second transistor (T2) is opened after the integration time has elapsed so that the signal is held at the conversion capacitor (C2) until the readout time and in that the first transistor (T1) or respectively the first diode (D1) is adjusted during this holding time so that the photodiode capacitor (C1) is not fully discharged.

11. The method as claimed in claim 10, characterized in that the gate voltage of the second transistor (T2) is adjusted during the reset phase and during the integration phase so that the gate voltage minus the threshold voltage is lower than the reset voltage which is set at the input of the readout amplifier (T3), and in that the gate voltage is higher than the saturation voltage of the readout buffer at least by a threshold voltage.

12. The method as claimed in one of claims 10 and 11, characterized in that the gate voltage of the second transistor (T2) is varied during the integration

phase, although it always remains greater than the gate voltage of the first transistor (T1), and in that the gate voltage of the first transistor (T1) is preferably reduced successively during the integration phase.

13. The method as claimed in one of claims 10 to 12, characterized in that the gate voltage of the first transistor (T1) is kept constant or successively reduced during the integration time.

14. The method as claimed in one of claims 10, 11 and 13, characterized in that the gate voltage of the second transistor (T2) is switched at least once so that it is equal to the bulk potential of this transistor (T2) and is switched back again to its original value.

15. A one- or two-dimensional array of optoelectronic sensors as claimed in one of claims 1 to 9.

16. A method according to one of claims 10 to 14 for operating an array as claimed in claim 15.